1/1

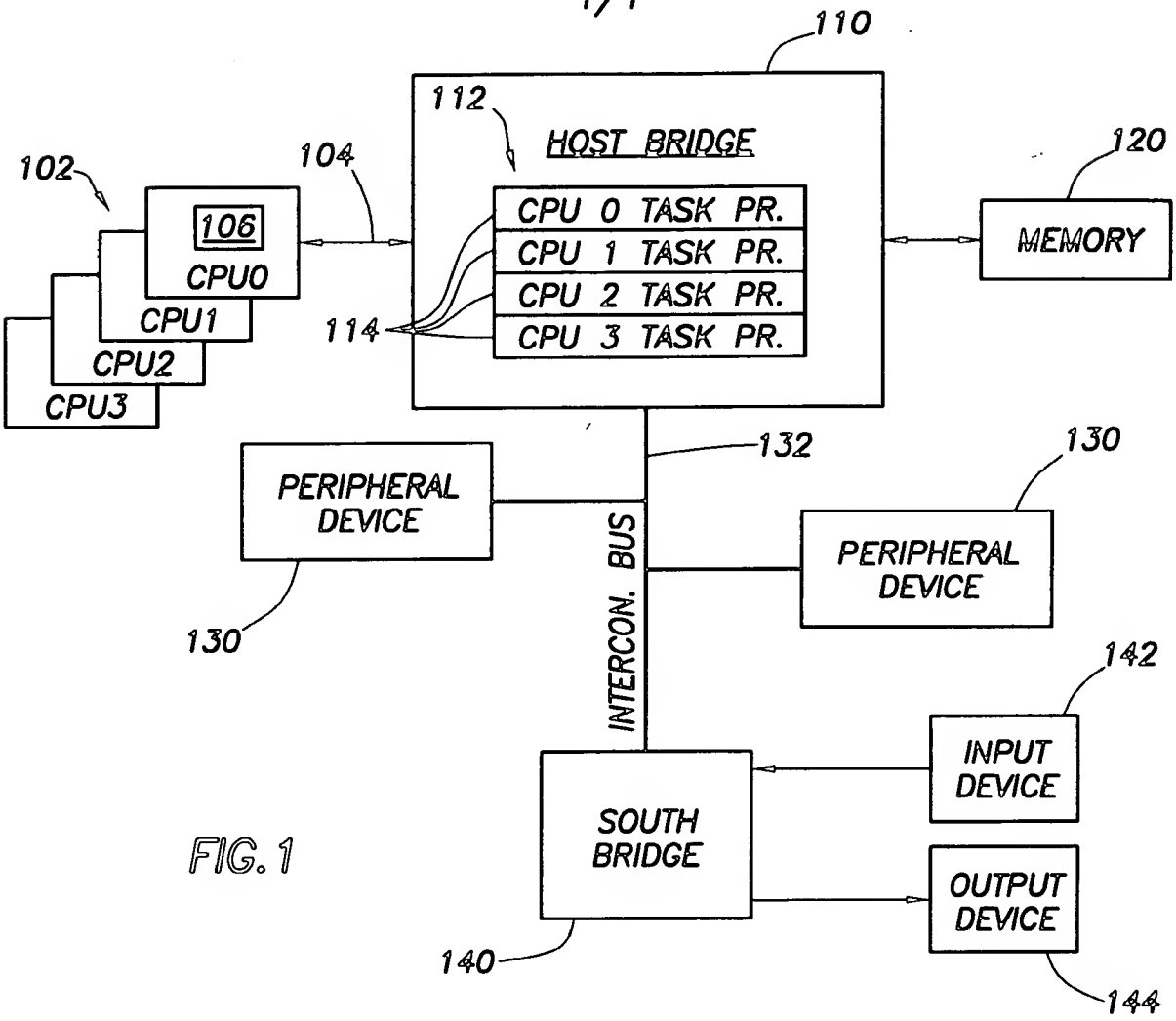
110
112
HOST BRIDGE
102
104
120
106
CPU0
CPU1
CPU2
CPU3
CPU 0 TASK PR.
CPU 1 TASK PR.
CPU 2 TASK PR.
CPU 3 TASK PR.
114
MEMORY
132
130
PERIPHERAL DEVICE
PERIPHERAL DEVICE
INTERCON. BUS
130
142
INPUT DEVICE
SOUTH BRIDGE
OUTPUT DEVICE
140
144

FIG. 1

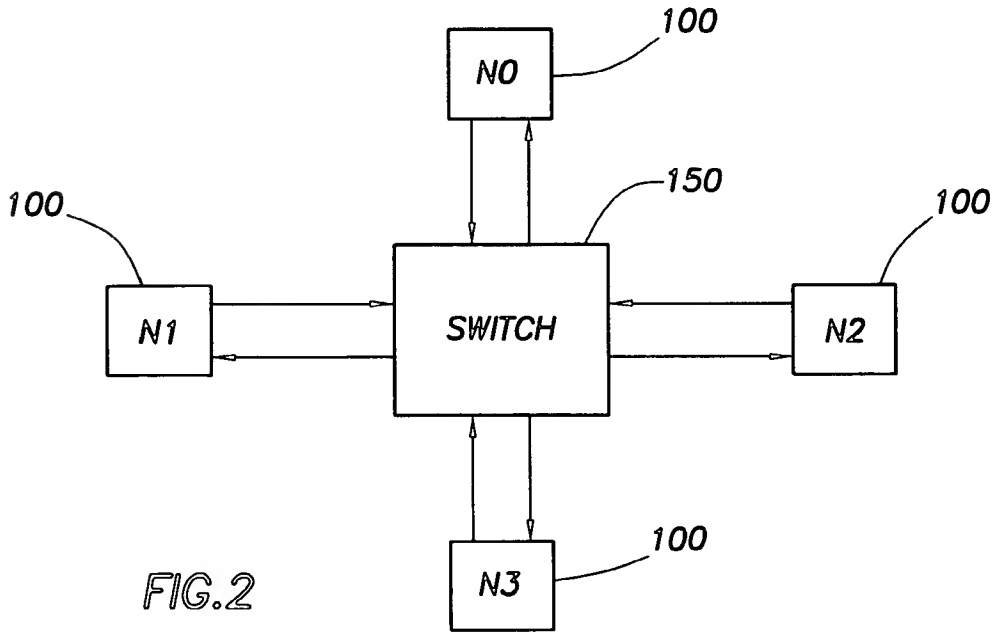
100
N0
150
100
100
N1
SWITCH
N2
100
N3

FIG. 2